1/2inch MCCD Sensor for PAL Color Video Cameras

BG0601D Datasheet

General Descriptions

BG0601D is a member of Brigates MCCD product Series.

BG0601D is a high performance ½ inch MCCD image sensor suitable for PAL color video cameras. This chip features high sensitivity and high dynamic range pixel compared with the conventional CCD image sensor.

Additionally, this chip also has on-chip advanced signal processing modules which remove fix pattern noise and improve image quality dramatically.

MCCD is mainly targeting high-end security & surveillance market.

MCCD Overview

MCCD denotes a type of image sensor which is fabricated with CMOS technology implementing compatible interface with CCD sensors. Like conventional CCD sensors, MCCD is a passive sensor, taking pulsed & driving signals from the DSP chip such as XV1~XV4, XH1, XH2, XSG, XSUB for the timing & controls. Unlike conventional CCD sensors：

- MCCD integrates PGA & A/D converters on-chip. It does not need external AFE and directly outputs digital signals.
- MCCD works with common CMOS 3.3V control signals. So HV driver is not need.
- MCCD integrated multiple interfaces for outside communications.
  - SPI Slave: connect DSP for gain control
  - SPI Master: connect SPI flash for sensor calibration.
  - I2C Master: connect EEPROM for initial setting.
  - I2C Slave: connect external host for internal register control.

  These interfaces enable MCCD to complete a variety of functions such as flexible image enhancement, gain control and etc. These functions are achieved thanks to the capability of the standard CMOS technology.

Table 1 MCCD/CCD comparison

Item	MCCD	CCD
PGA & A/D converter	Build in	No, need external
On chip digital circuit	FPN Removal, BLCC and etc.	No
Communication	SPI I2C	No
Data output	Digital	Analog
Driving Voltage	Low Voltage	High voltage
High light vertical overflow	No	Yes
Infrared performance	Prominent	Normal

MCCD Camera Buildup

MCCD camera is used as the essential part of a camera system which also need DSP as the timing & control generator, image processor and eventually output CVBS video signal for monitor display.

As mentioned above, MCCD works with CMOS 3.3V environment and incorporates PGA and A/D Converters. There is no need to add analog front end and high voltage driver chips in the application system. Besides, MCCD provides SPI and I2C interface for system control and data exchange which make the system more flexible and powerful. Figure 1 shows the difference of the build up for both MCCD and CCD applications.

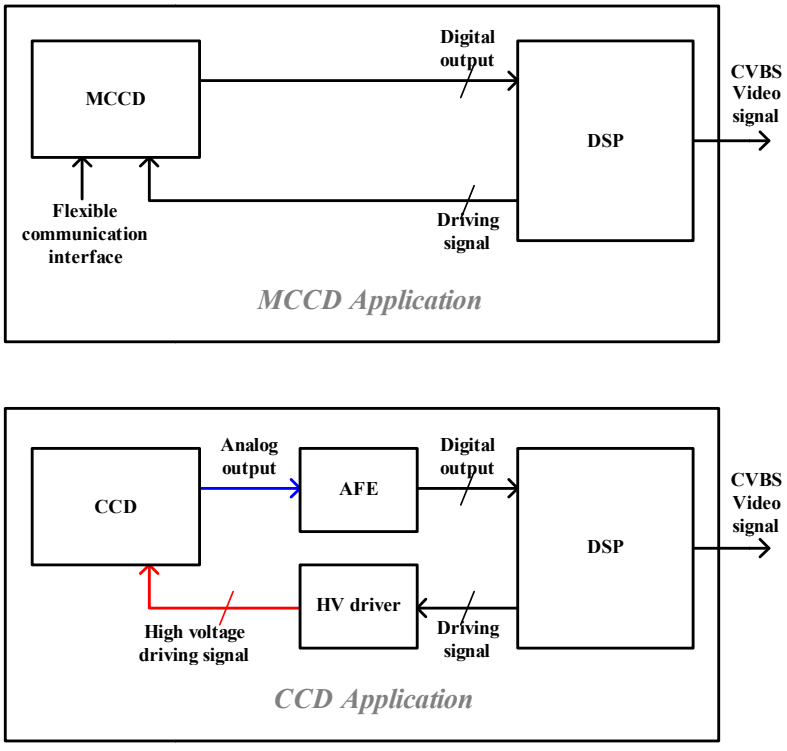

Figure 1 Common Buildup of MCCD & CCD Application System

Table of Content

List of Figures

List of Tables

Features

- CCD compatible control interface.
- High sensitivity and high dynamic range pixel
- CMYG color filter array
- Build-in PGA&AD converter.
- Superior low light performance.
- Enhanced NIR performance.
- Auto black level calibration.
- On-chip FPN removal.
- 2-wire serial control interface.
- Easy connection with security DSP chip for conventional CCD camera.

Key Parameter

Table 2 Key Specification

Parameter		Typical Value
Optical format		1/2 inch
Active pixel array		768H x 582V
Pixel size		8.60um(H) x 8.30um(V)
Active pixel array Area		6604.8 um x 4830.6 um
Frame rate		50fps@PAL
Color filter array		Complementary Bayer
Shutter Type		Electronic Rolling
SNR		48dB
Dynamic range		69dB
Output		10-bit
Power supply	Digital	Internal 1.8v
	IO	3.0V ~3.45V
	Analog	3.15V ~3.45V
Power Consumption		280mW@PAL
Package Option		48 pin CLCC

Top-level Description

The functional diagram of BG0601D is shown as Figure 2.

BG0601D is a MCCD image sensor with 768x582 active pixels array. The timing and control circuitry receives frame reset and frame readout signals (XSUB, XSG) to generate the column/row driver signals, which sequence through the rows of array, resetting and then reading each row in turn. Once the pixel data of a row is put onto bit-line, analog processing (providing CDS and gain) and A/D conversion is performed in column parallel way. The output from the ADC is a 10-bit value for each pixel.

Digital image processing unit mainly deal with the fix pattern noise cancellation (including column wise fix pattern noise and dark current noise) and row wise noise removal. Besides, digital gain is performed in this part. After that, image data will output in parallel by the control of horizontal transfer signal (H1, H2).

Figure 3 shows the driving signal diagram, and Figure 4 shows parallel output timing diagram.

BG0601D utilized SPI and I2C interface for system control and data exchange. SPI slave is used to receive gain code for the gain control unit. SPI master is used to connect off-chip flash which serves the digital image processing unit. I2C master should be connected to the off-chip EEPROM to load the initial setting. I2C slave interface connects external host to access to the internal register file.

Typical connection diagram is shown as Figure 5. Common CCD DSP (i.e. NVP2040e) provides scan control signals, SPI slave bus signals and main clock of BG0601D. Under the control of DSP, BG0601D will output 10-bit digital value of pixels with the proper timing and gain. Off-chip FLASH is connected through the SPI master interface to serves the digital image processing unit. Off-chip EEPROM is connected through the I2C master interface to load the initial setting. Besides, BG0601D's I2C slave interface can be connected for adjustment usage. Both I2C master and I2C slave need pull-up resistance.

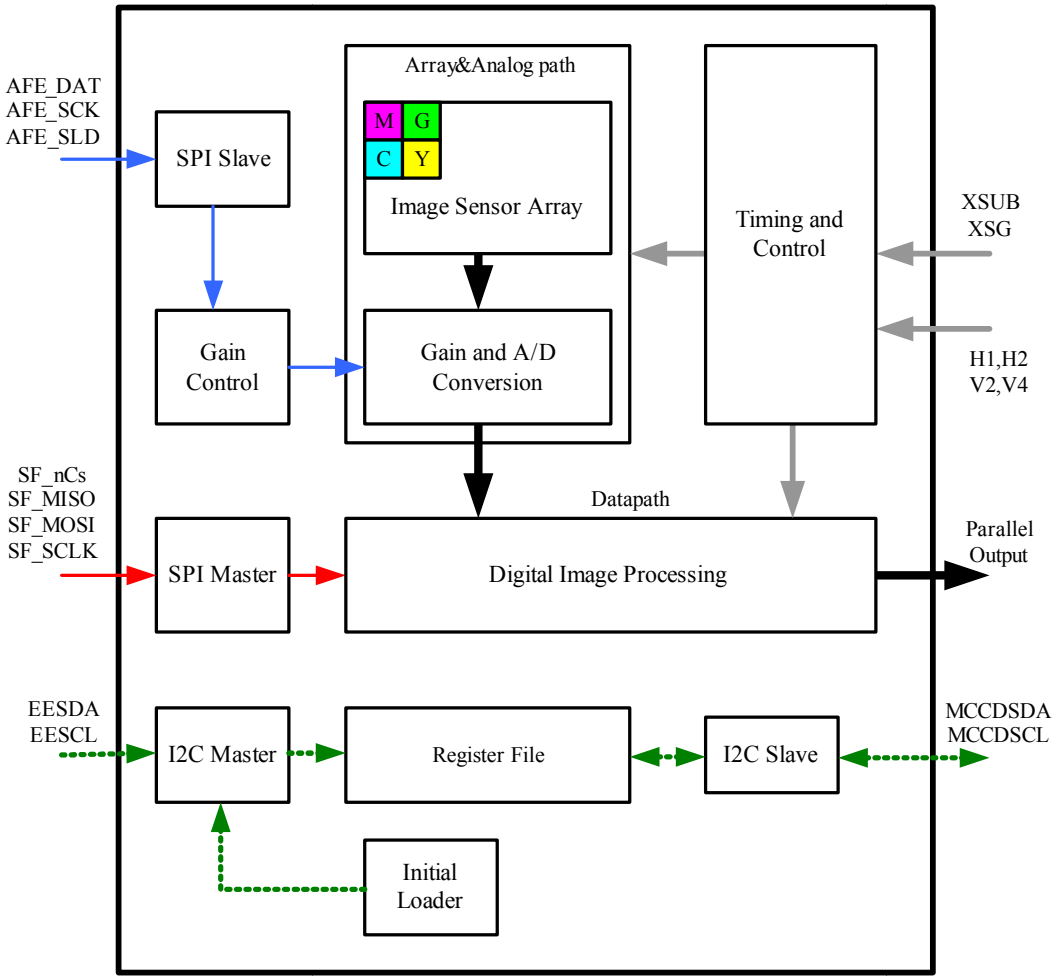

Figure 2 Block Diagram

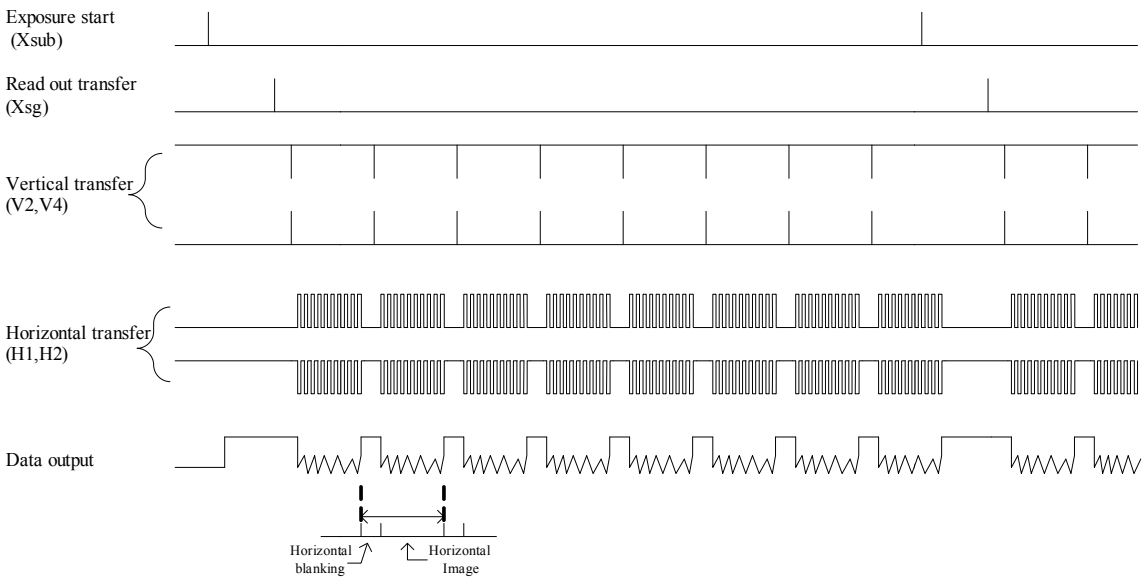

Figure 3 Driving Signal Diagram

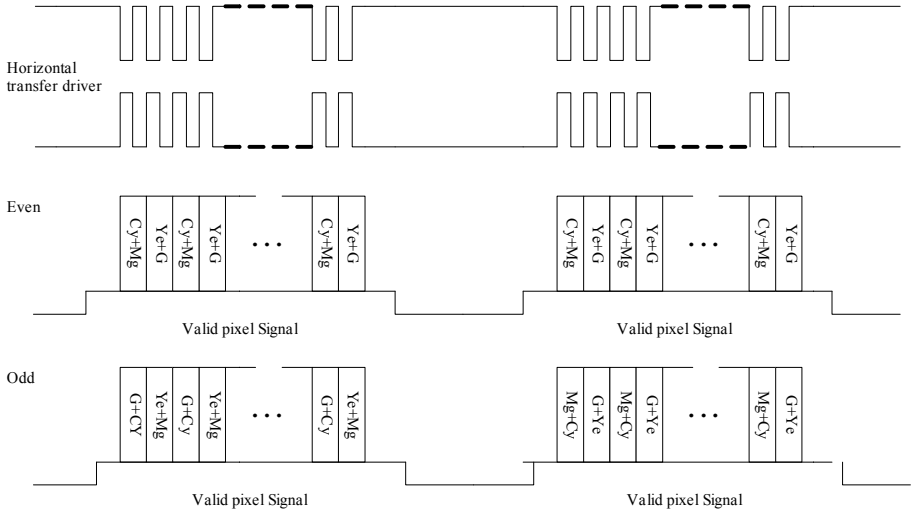

Figure 4 Even and Odd Data Output Timing

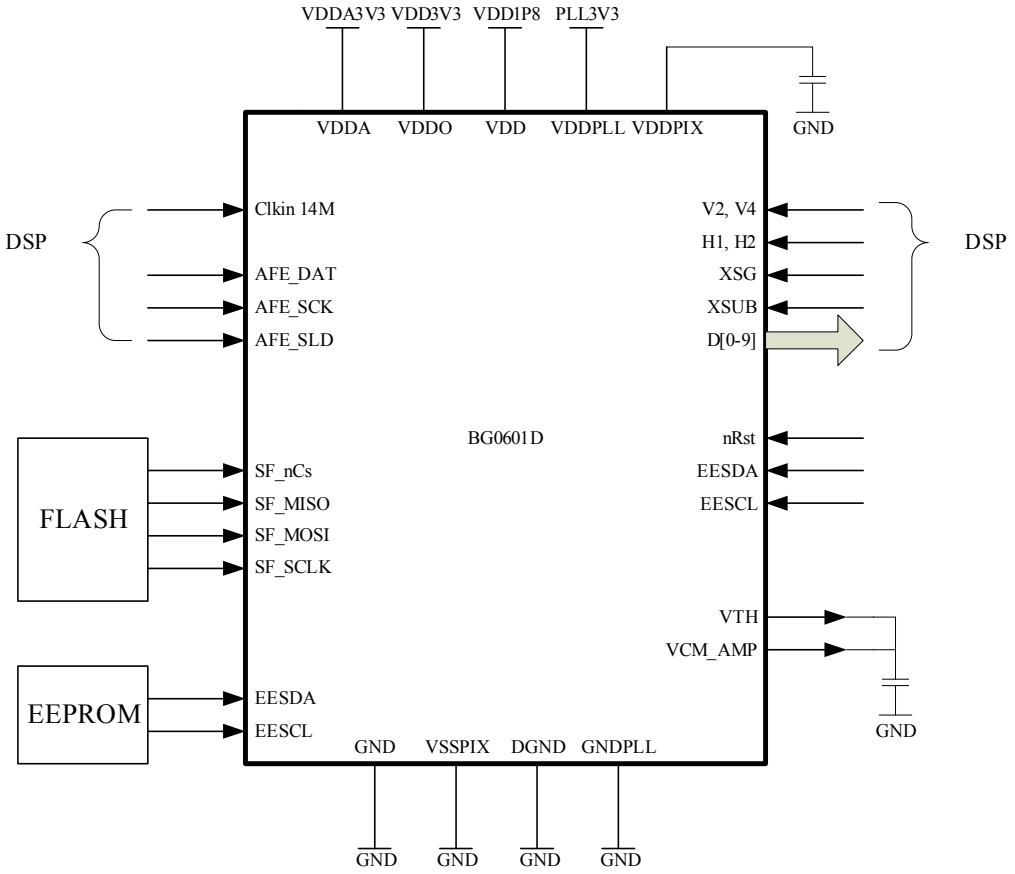

Figure 5 Typical Connection Diagram

Block-level Description

Image Sensor Array

The image sensor array contains 768 x 582 active pixels. Besides, 6 dark rows and 36 dark columns as Figure 6 can be read out for special purpose. BG0601D employs complementary color filter of CYMG (cyan, yellow, magenta and green), the color filter arrangement (top right corner of array) is show in Figure 7.

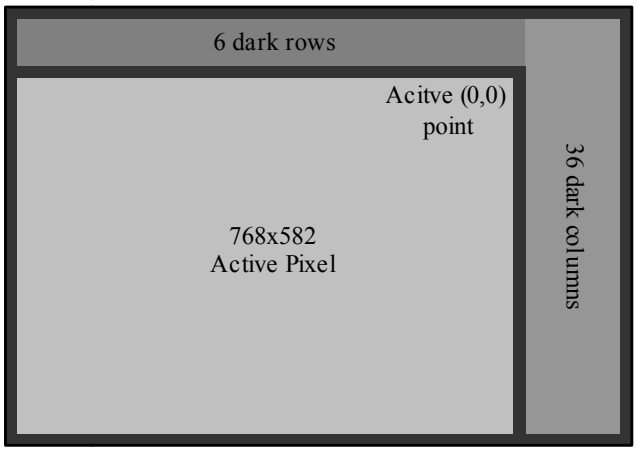

Figure 6 Pixel Array Read Out

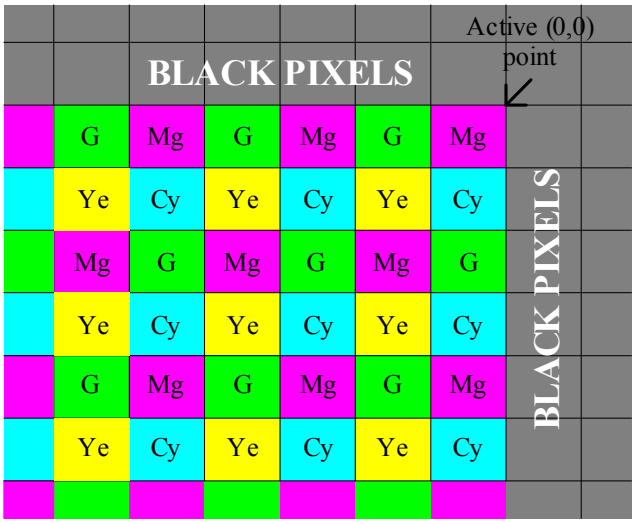

Figure 7 Color Filter Arrangements

I2C Master Interface

BG0601D utilizes I2C master interface to load initial settings from off-chip EEPROM. It will read the off-chip EEPROM at the power up phrase. Maximum support EEPROM is 16K size.

I2C Slave Interface

BG0601D is programmable through I2C interface with reading slave device address 0x65 and writing slave device address 0x64. The related IO pin is MCCDSCL and MCCDSDA. MCCDSCL works as the serial clock and MCCD as the data line.

Figure 8 shows example of the write operation (Writing 0x2C register with 0x56 data). The sequence is defined as following:

- The master sends a start bit to the slave.
- The master sends the slave device address with write mode.
- The slave sends an acknowledge bit to the master to indicate receive its slave device address.
- The master sends 8-bit register address to the slave.
- The slave sends an acknowledge bit after it receives the 8-bit data.
- The master sends 8-bit register data to the salve.
- The slave sends an acknowledge bit after it receives the 8-bit data
- The master sends a stop bit to the slave.

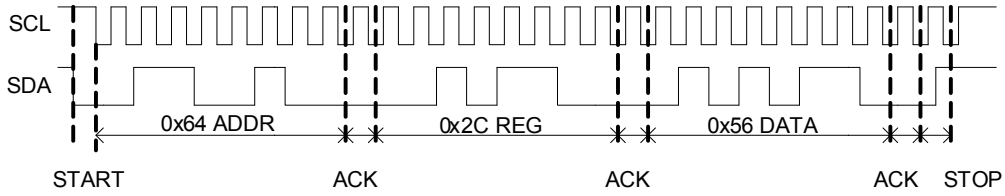

Figure 8 I2C Slave Write Operation

Figure 9 shows example of the read operation (Writing 0x56 data from 0x2C register). The sequence is defined as following:

- The master sends a start bit to the slave.
- The master sends the slave device address with write mode.
- The slave sends an acknowledge bit to the master.
- The master sends 8-bit register address to the slave.
- The slave sends an acknowledge bit to the master.
- The master sends a start bit to the slave.
- The master sends the slave device address with read mode.
- The slave sends an acknowledge bit to the master.
- The slave sends 8-bit data to the master
- The master sends a no-acknowledge bit to the slave.
- The master sends a stop bit to the slave to stopping read.

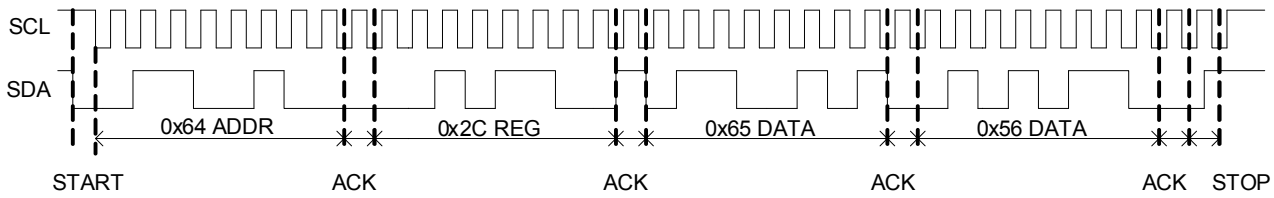

Figure 9 I2C Slave Read Operation

SPI Master Interface

BG0601D SPI master interface supports Dual IO Mode (cmd=0xBB) which outputs address by SF_MOSI and SF_MISO, and Dual Output Mode (cmd=0x3B) which outputs address by SF_MOSI only. Both of these two modes use SF_MOSI and SF_MISO to transfer data.

SPI Slave Interface

Figure 10 shows serial write operation of SPI flash which transfer VGA code for gain control.

1. AFE_SDA Bits are internally latched on the rising edges of AFE_SCK.
2. System update of loaded registers occurs on AFE_SLD rising edge.
3. All 12 data bits D0-D11 must be written. If the register contains fewer than 12 bits, zeros should be used for the undefined bits.
4. Test bit is for internal use only and must be set low.

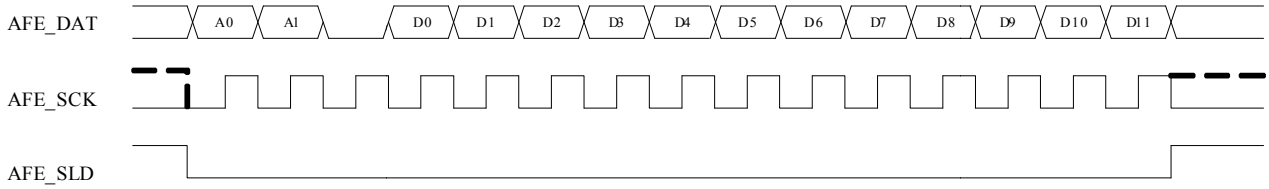

Figure 10 Serial Write Operation

Timing and Control

The timing and control circuitry receives frame reset and frame readout signals (XSUB, XSG) to generate the column/row driver signals, which sequence through the rows of array, resetting and then reading each row in turn.

Gain Control

Gain control unit receives gain code through SPI slave interface from DSP. According to the gain code, it assures the pixel output with proper gain amplified.

Digital Image Processing

Digital Image processing unit focuses on three type of noise: row wise noise, column wise fix pattern noise and dark current noise.

- Row wise noise correction:
  Row wise noise is handled automatically by the image sensor. Row wise noise correction unit measures a set of optical black pixels at the start of each line and then apply the average to the tied active pixels of the line.
- Column wise fix pattern noise correction:
  To achieve fast frame rate, BG0601D uses column parallel readout architecture. Column wise fix pattern noise correction unit is used to correct the difference caused by the different column signal path. To use this feature, fix pattern

column noise should be measured first by set the integration time to 0 and capture the image output. Besides, off chip flash is needed to storage the noise data. Specified tool is provided to process this operation.

- Dark current noise correction:
  BG0601D use dark current noise correction function to remove dark current precisely. This feature also need calibration and off chip flash. Specified tool is provided to process this operation.

Initial Loader

BG0601D use an initial loader to load the necessary setting at the power up phrase. The necessary setting is stored in the off chip EEPROM connected to the I2C master.

Pin Outs

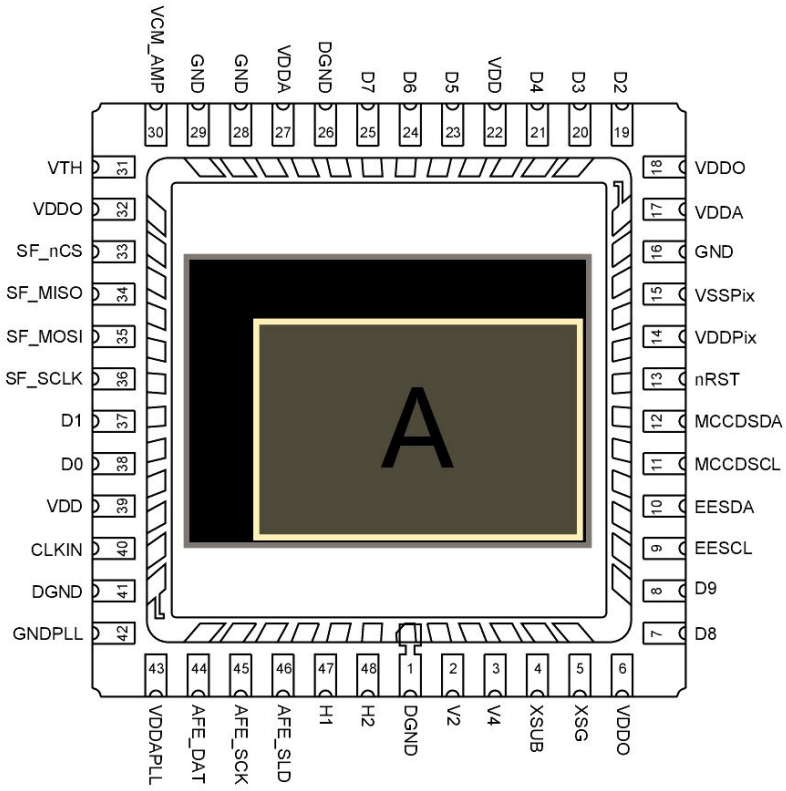

Figure 11 48-Pin PLCC Pinout Diagram

Table 3 IO Description

PIN NO.	NAME	I/O	TYPE	DESCRIPTION
1	DGND	–	P	Digital Ground
2	V2	I	D	Vertical Transfer Clock
3	V4	I	D	Vertical Transfer Clock

4	XSUB	I	D	Discharge Pulse
5	XSG	I	D	Sensor Charge Readout Pulse
6	VDDO	–	P	I/O Power
7	D8	O	D	Pixel Data Out Bit8
8	D9	O	D	Pixel Data Out Bit9
9	EESCL	I/O	D	Master Serial Bus Clock.
10	EESDA	I/O	D	Master Serial Bus Data.
11	MCCDSCL	I/O	D	Slave Serial Bus Clock
12	MCCDSDA	I/O	D	Slave Serial Bus Data
13	nRST	–	A	Power On Reset
14	VDDPIX	–	P	Pixel Array Power
15	VSSPIX	–	P	Pixel Array Ground
16	VSSA	–	P	Analog Ground
17	VDDA	–	P	Analog Power
18	VDDO	–	P	I/O Power
19	D2	O	D	Pixel Data Out Bit2
20	D3	O	D	Pixel Data Out Bit3
21	D4	O	D	Pixel Data Out Bit4
22	VDD	–	P	Digital Core Power
23	D5	O	Out	Pixel Data Out Bit5
24	D6	O	Out	Pixel Data Out Bit6
25	D7	O	Out	Pixel Data Out Bit7
26	DGND	–	P	Digital Ground
27	VDDA	–	P	Analog Power
28	VSSA	–	P	Analog Ground
29	VSSA	–	P	Analog Ground
30	VCM_AMP	–	A	Analog Bias
31	VTH	–	A	Charge Pump Out
32	VDDO	–	P	I/O Power
33	SF_nCS	O	D	SPI Master Chip Select

34	SF_MISO	I/O	D	SPI Master MISO
35	SF_MOSI	I/O	D	SPI Master MISO
36	SF_SCLK	O	D	SPI Master CLK
37	D1	O	D	Pixel Data Out Bit1
38	D0	O	D	Pixel Data Out Bit0
39	VDD	–	P	Digital Core Power
40	CLKIN	I	D	Clock Input.
41	DGND	–	P	Digital Core Ground
42	VSSPLL	–	P	PLL Ground
43	VDDPLL	–	P	PLL Power
44	AFE_DAT	I	D	Slave SPI Input
45	AFE_SCK	I	D	Slave SPI Clock
46	AFE_SLD	I	D	Slave SPI Chip Select
47	H1	I	D	Horizontal Transfer Clock
48	H2	I	D	Horizontal Transfer Clock

Chip Control

Gain

BG0601D has three stages of gain, including PGA gain, AD Ramp gain and Digital gain. Gain control unit receives gain code through SPI slave interface from DSP. And then VGA code is mapped into PGA gain, Ramp gain and digital gain.

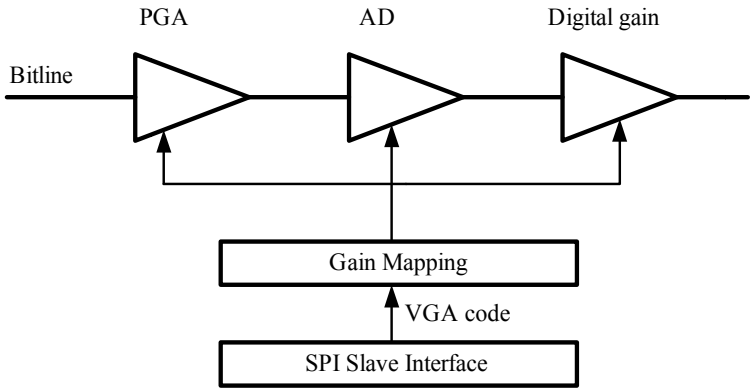

Figure 12 Analog Processing and AD Conversion

- PGA Gain:
  BG0601D has a column parallel architecture and it has an analog gain stage per column. PGA gain can be controlled by register C_s and C_f (0xb4, 0xb5 on page 00). The PGA Gain is determined by:
  $Gain_{pga} = C_s / C_f$
  The maximum PGA gain is 16x.
- Ramp Gain:
  Ramp Gain controls the slope of AD ramp. It's control by register 0xb6 on Page 00.
- Digital Gain:
  Digital gain can be controlled by register 0xb7 and 0xb8 on page 00. The format for digital gain setting is x_xxx_xxx.yyy_yyy_yy where 16'h0200 represents a 1x gain.

PLL

The BG0601D has an internal PLL, which can generate PLL clock (f_{out}) 100MHz~250MHz.

The PLL is controlled through its PLM, PLN and PLK parameters. The PLL output frequency (f_{out}) has the following relationship to the input frequency (f_{xclk}):
$f_{out} = f_{xclk}*(PLM+2)/((PLN[5:0]+2)*PLLK)$

Note:
1) PLM=0~127;

2) PLN=0~63;
3) PLK[1:0]=2'b00: PLLK=2
PLK[1:0]=2'b01: PLLK=4
PLK[1:0]=2'b10: PLLK=8
PLK[1:0]=2'b11: PLLK=16

The input clock should be 14.1M and the Default frequency is 91M with PLM=63 PLN=3 and PLLK=2.
The PLL takes time to power up. During this time, the behavior of its output clock is not guaranteed.

The PLL can be bypassed manually. When the PLL has been bypassed, the input clock will be set as the main clock.

Chip Characteristics

Opto-electrical Characteristics

Table 4 Opto-electrical Characteristics

Item	Symbol	Min	Typ	Max	Unit	Remarks
Sensitivity	S		5800		mV	
Sensitivity ratio	RMgG		1.13			
	RYeCy		1.54			
Saturation signal	Ysat	1250		1400	mV	Ta=60℃
Smear	Sm		-118	-116	dB	
Video signal shading	Shy			20	%	Zone 0 to I
				25	%	Zone 0 to II
Uniformity between video signal channels	ΔSr			10	%	
	ΔSb			10	%	
Dark signal	Ydt			4	mV	Ta=60℃
Dark signal shading	ΔYdt			2	mV	Ta=60℃
Flicker Y	Fy			2	%	
Flicker R-Y	Fcr			5	%	
Flicker B-Y	Fcb			5	%	
Line craw R	Lcr			3	%	
Line craw G	Lcg			3	%	
Line craw B	Lcb			3	%	
Line craw W	Lcw			3	%	
Lag	Lag			0.5	%	

Notice: Due to the cosmic radiation, pixels of CMOS image sensor may be distorted and cause white point effect in dark signals. This process happens slowly, but unfortunately current scientific technology can not remove this effect totally. It is recommended that automatic compensation system for white pixels should be adopted in the application.

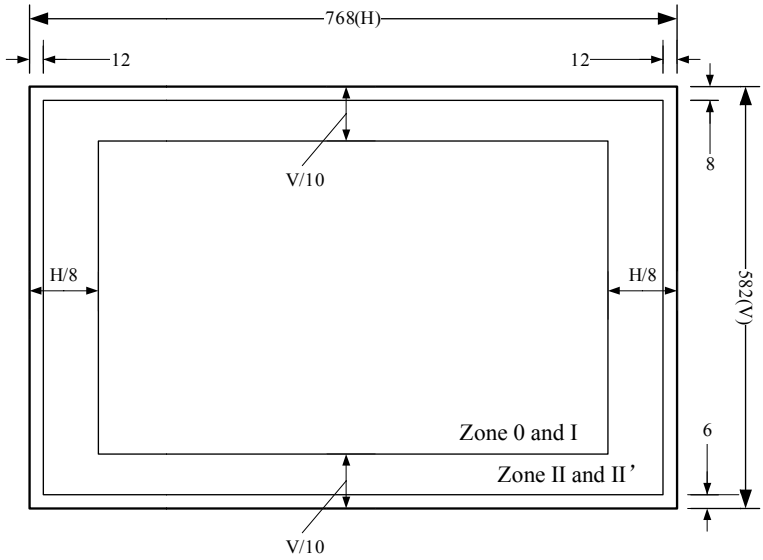

Figure 13 Zone Definition of Video Signal Shading

Spectral Responsivity

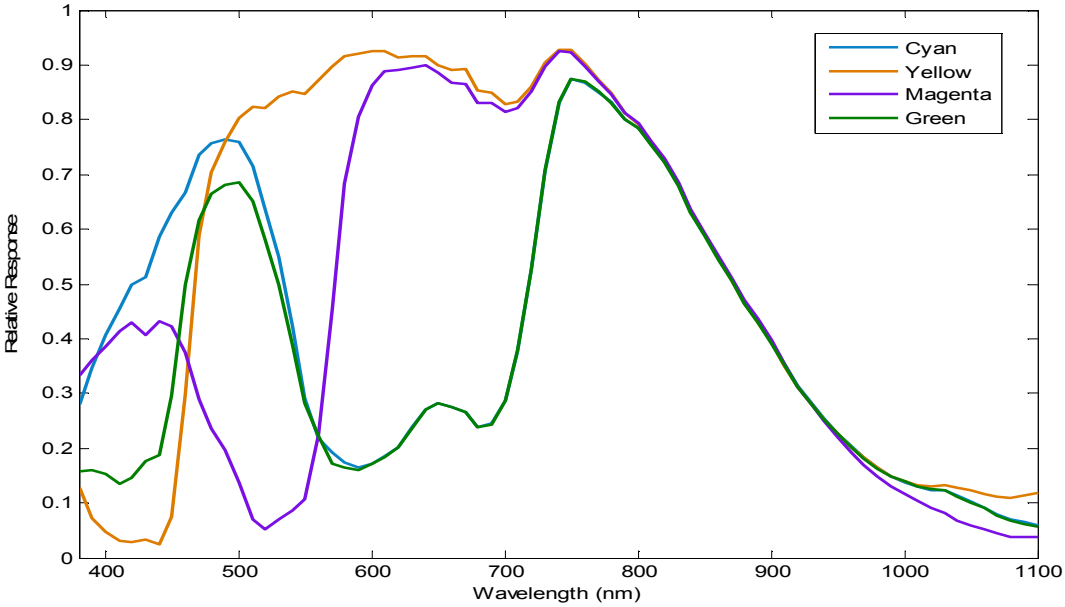

Figure 14 Spectral Responsivity

I/O Timing

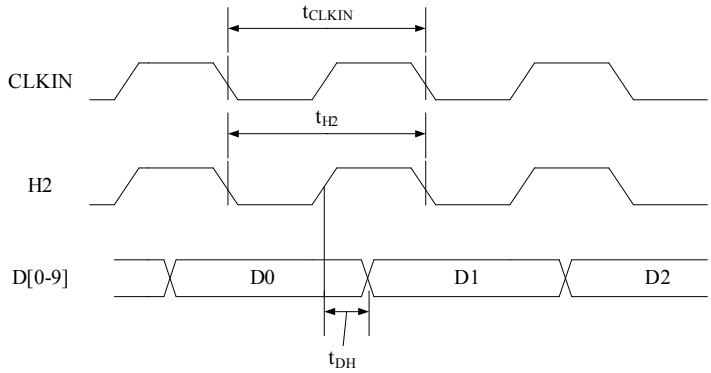

Figure 15 I/O Timing Diagram

Table 5 IO Timing

Symbol	Definition	Min	Typ	Max	Unit
t_{CLKIN}	Input clock period		70		ns
t_{H2}	Input clock period		70		ns
t_{DH}	D[0-0] hold time	31.8		36.8	ns

Electrical Specifications

Table 6 Electrical Specification

Symbol	Definition	Condition	Min	Typ	Max	Unit	Note
V_{DD-A}	VDDA voltage		3.15	3.3	3.45	V	
V_{DD-D}	VDD voltage		1.7	1.8	1.9	V	
V_{DD-IO}	VDDO voltage		3.0	3.3	3.6	V	
V_{IH}	Input Voltage High		0.7 *V_{DD-IO}			V	
V_{IL}	Input Voltage Low				0.3 *V_{DD-IO}	V	
I_{IN}	Input Leakage Current	No pull-up resistor ,VIN=V_{DD-IO} or DGND	-1		1	μA	
V_{OH}	Output High Voltage		0.9 *V_{DD-IO}			V	
V_{OL}	Output Low Voltage				0.1*V_{DD-IO}	V	
I_{OH}	Output Current High	V_{OH}=0.9*V_{DD-IO}	-7			mA	
I_{OL}	Output Current Low	V_{OH}=0.1*V_{DD-IO}	-7			mA	
I_{DD-A}	Analog Operating Current	f_{PCLK}=14.1 MHz Default setting		70		mA	
I_{DD-D}	Digital Operating Current	f_{PCLK}=14.1 MHz Default setting		31		mA	
I_{DD-IO}	IO Operating Current	f_{PCLK}=14.1 MHz Default setting		1.5		mA	

Maximum Ratings

Table 7 Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage(analog 3.3)	V_{DD-A}	−0.3	4.0	V	
Supply voltage(analog 3.3)	V_{DD-IO}	−0.3	4.0	V	
Supply voltage(digital 1.8)	V_{DD-D}	−0.3	2.5	V	
Input voltage	VI	−0.3	V_{DD_IO}+0.3	V	Not exceed 3.3 V
Output voltage	VO	−0.3	V_{DD_IO}+0.3	V	Not exceed 3.3 V
Operating temperature	T_{opr}	−30	+70	℃	
Storage temperate	T_{stg}	−30	+80	℃	

Power-up Sequence

The recommended power up sequence is show in Figure 16.

1. Turn on VDDO, VDDA, VDD and VDDPIX power supply.
2. After 10ms pull up RSTB.
3. Wait 10ms to supply CLKIN.

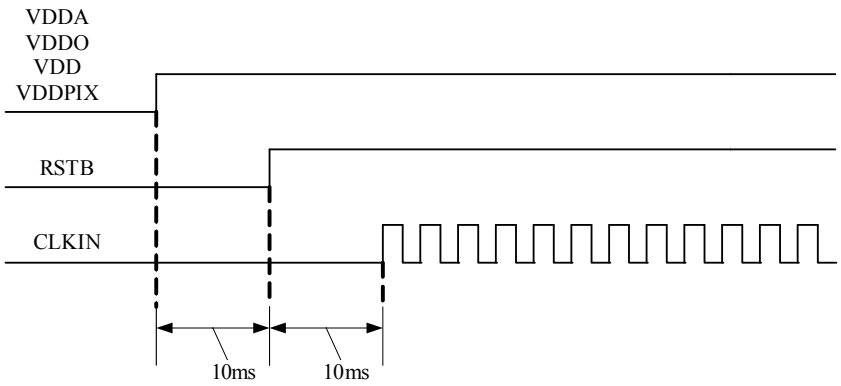

Figure 16 Power-up Sequence