Hi3516E V200 Economical HD IP Camera SoC

Brief Data Sheet

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Hi3516E V200 Economical HD IP Camera SoC

Major Specifications

Processor Core

- ARM Cortex-A7@ 900 MHz, 32KB I-Cache, 32KB D-Cache /128KB L2 cache
- NEON acceleration and the integrated floating-point processing unit (FPU)

Video Encoding

- H.264 BP/MP/HP, supporting I-/P- frames
- H.265 MP, supporting I-/P- frames
- MJPEG/JPEG baseline encoding

Video Encoding Performance

- Maximum resolution for H.264 /H.265 encoding: 2304 x 1296 (with the width up to 2304)
- Real-time multi-stream H.264/H.265 encoding capability:
  - 2048 x 1536@20 fps + 720 x 576@20 fps
  - 2304 x 1296@20 fps + 720 x 576@20 fps
  - 1920 x 1080@30 fps + 720 x 576@30 fps
- JPEG snapshot at 3M (2304 x 1296)@5 fps
- CBR, VBR, FIXQP, AVBR, QPMAP and CVBR bit rate control modes
- Intelligent encoding mode
- Up to 60 Mbit/s output bit rate
- Encoding of eight ROIs

Intelligent Video Analysis

- IVE
- Various intelligent analysis applications, such as intelligent motion detection, perimeter defense, and video diagnosis

Video and Graphics Processing

- 3DNR, image enhancement, and DCI
- Anti-flicker for output videos and graphics
- 1/15x to 16x video and graphics scaling
- Overlaying of videos and graphics
- Image rotation by 90°, 180°, or 270°
- Image mirror and flip
- OSD overlaying of eight regions before encoding

ISP

- 4 x 4 pattern RGB-IR sensor
- 3A (AE, AF, and AWB) function. The third-party 3A algorithms are supported.
- FPN removal and DPC
- LSC, LDC, and purple edge correction
- Direction-adaptive demosaic
- Gamma correction, DCI, and color management and enhancement
- Adaptive region de-fog
- Multi-level NR (BayerNR and 3DNR) and sharpening enhancement
- Local tone mapping
- Sensor built-in WDR
- 2F-WDR frame-based mode
- DIS
- Intelligent ISP tuning and ISP tuning tools for the PC

Audio Encoding and Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Compliance with the G.711, G.726, and ADPCM protocols
- Audio 3A functions (AEC, ANR, and AGC)

Security Engine

- AES/RSA encryption and decryption algorithms implemented by using hardware
- HASH (SHA1/SHA256/HMAC_SHA1/HMAC_SHA256) algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and random number generator

Video Interfaces

- Input
  - 8-/10-/12-bit RGB Bayer DC timing VI
  - MIPI, LVDS/sub-LVDS, and HiSPi
  - Compatibility with mainstream HD CMOS sensors provided by Sony, ON, OmniVision, and Panasonic
  - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
  - Programmable sensor clock output
  - Maximum input resolution: 2304 x 1296
- Output
  - 6-/8-bit LCD output
  - BT.656/BT.1120 output

Audio Interfaces

- Integrated audio codec, supporting 16-bit audio input and output
- Mono MIC/line-in input
- Mono line-out output
- I^2S interface for connecting to external audio codec

Peripheral Interfaces

- POR
- Integrated high-precision RTC
- Integrated 2-channel LSADC
- Three UART interfaces
- I^2C, SPI, and GPIO interfaces
- Four PWM interfaces
- One SDIO 2.0 interface and one SD 2.0 card
- One USB 2.0 host/device port
- Integrate FE PHY. TSO network acceleration is supported.

External Memory Interfaces

- SDRAM interface
  - Built-in 512 Mb DDR2
- SPI NOR flash interface

  - 1-/2-/4-line mode
  - Maximum capacity: 256 MB
- SPI NAND flash interface
  - 1-/2-/4-line mode
  - Maximum capacity: 1 GB
- eMMC 4.5 interface
  - 4-bit data width

Boot

- Booting from the SPI NOR flash memory, SPI NAND flash memory, or eMMC
- Secure boot

SDK

- Huawei LiteOS/Linux-4.9-based SDK
- High-performance H.264 PC decoding library
- High-performance H.265 PC, Android, and iOS decoding libraries

Physical Specifications

- Power consumption
  - Typical power consumption in the 1080P30/3M20 scenario: 700 mW
- Operating voltages
  - 0.9 V core voltage
  - 3.3 V I/O voltage (±10%)
  - 1.8 V SDRAM interface voltage
- Packaging
  - 9 mm x 9 mm, 88 pins, 0.35 mm ball pitch, QFN package

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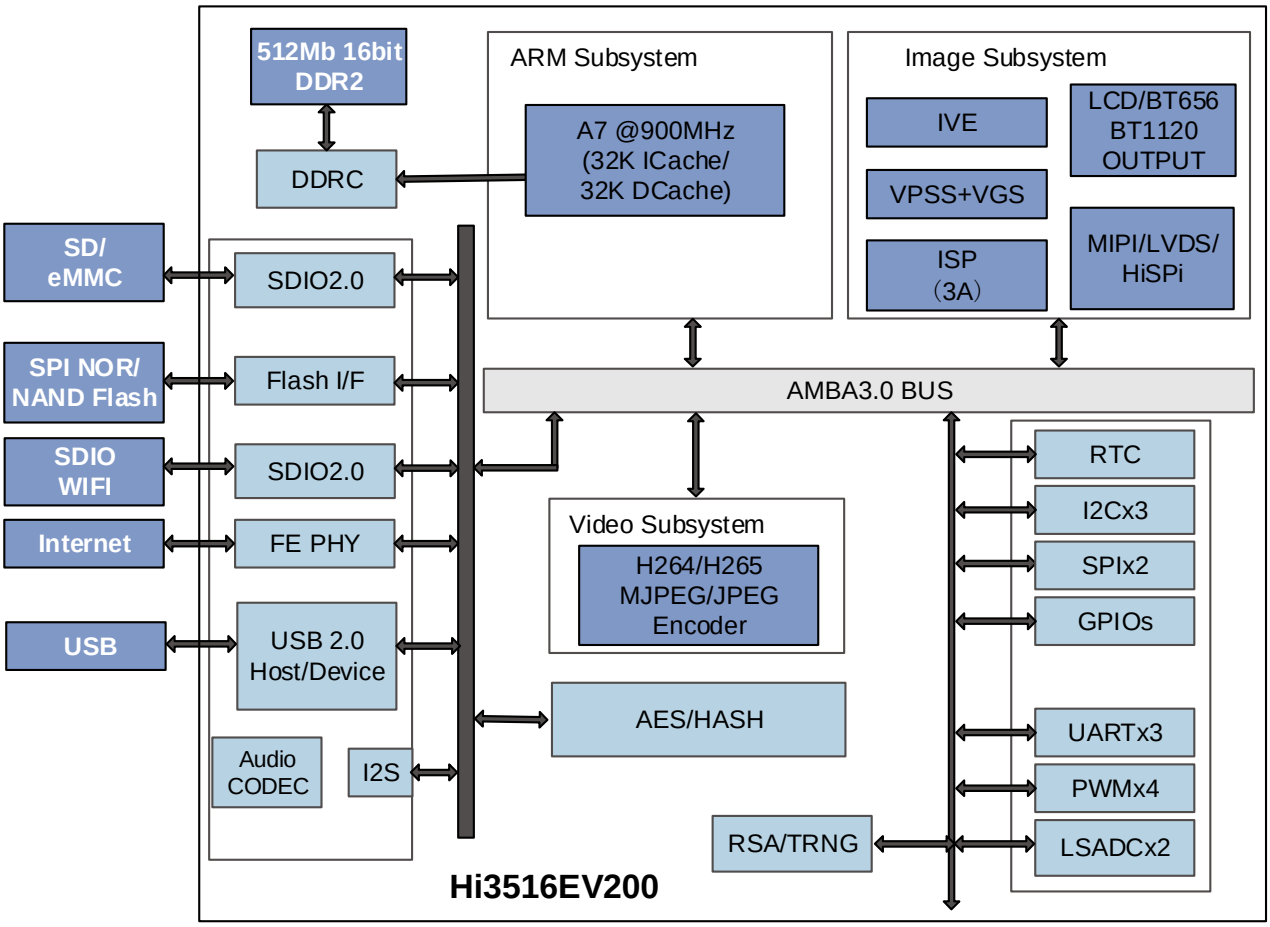
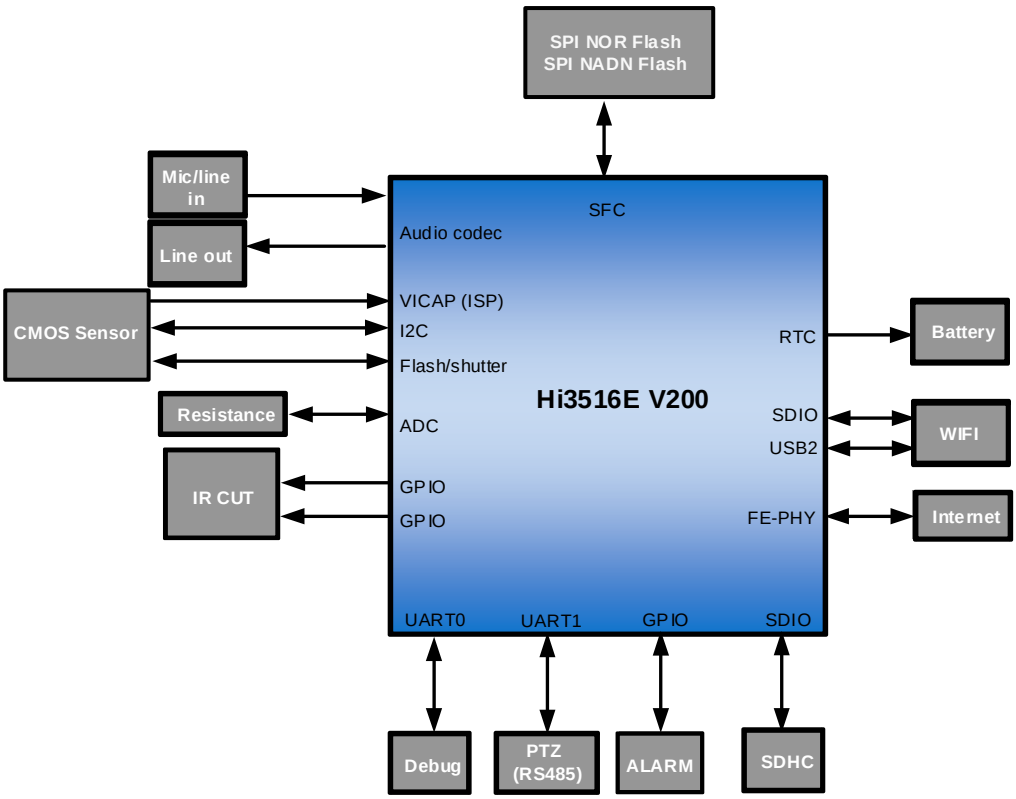
Functional Block Diagram



Hi3516E V200 is a new-generation SoC designed for the industry-dedicated HD IP camera. It has an integrated new-generation ISP and the latest H.265 video compression encoder in the industry. It uses the advanced low-power technology and architecture design. All of these features enable Hi3516E V200 to lead the industry in the low bit rate, high picture quality, and low power consumption. The POR, RTC, and audio codec are integrated to greatly reduce the EBOM cost. Hi3516E V200 also provides similar interface designs to the HiSilicon DVR and NVR SoCs, facilitating rapid mass production.

Hi3516E V200 HD IP Camera Solution



Acronyms and Abbreviations

3DNR	three-dimensional noise reduction
BP	Baseline Profile
AE	automatic exposure
AES	advanced encryption standard
AF	auto focus
AWB	automatic white balance
CBR	constant bit rate
DDR	double data rate
DES	data encryption standard
DIS	digital image stabilization
EBOM	engineering bill of materials
HD	high definition
HDMI	high definition multimedia interface
HiSPi	high-speed serial pixel interface
HP	High Profile
IR	infrared spectrum
ISP	image signal processor
IVE	intelligent video engine
LSADC	low-speed analog-to-digital converter
LSC	lens shading correction
LVDS	low-voltage differential signaling

MIC	microphone
MIPI	mobile industry processor interface
MP	Main Profile
NR	noise reduction
OSD	on-screen display
OTP	one-time programmable
POR	power-on reset
PWM	pulse-width modulation
QFN	Quad Flat No-lead Package
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SDIO	secure digital input output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system on a chip
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VI	video input
VO	video output
WDR	wide dynamic range